Course Syllabus for CSE-424

1. Title: Digital System Design (Sessional) **Course Code:** CSE-424

2. Credits: 1.5 (3 hours of lab work per week) **Session:** 2018-19

3. Course Teacher: Dr. Asaduzzaman, Professor, Dept. of CSE, CUET
Md. Billal Hossain, Lecturer, Dept. of CSE, CUET

4. Learning Resources:

Textbook(s): Morris Mano, Charles R. Kime, Madison; Tom Martin, -- Logic and computer design fundamentals, FIFTH EDITION (2015) Pearson

Reference:

Alan B. Marcovitz,-- Introduction to Logic Design, Third Edition, McGraw-Hill

M. Morris Mano and Michael D. Ciletti, -- Digital Design with an Introduction to the Verilog HDL (FIFTH EDITION, 2015), Pearson

5. Catalog Description: Sessional based on the following topics:

Register transfer logic, Hardware description language, inter register transfer, bus transfer, memory transfer, microoperations and macrooperations, design of bus systems, representation of digital data in registers and memory, design of a simple computer. Processor organization, design of arithmetic logic unit (ALU), status register, design of shifter, design of processor unit, design of accumulator. Control Logic Design, Control organization, Design of hardwire and software control, Micro-program sequencer. Computer Design with a given System configuration: Instruction set, Programming, Fetch cycle, Execution cycle, Design of computer registers, Design of control, Bus buffer and memory cycle of microcomputers. Design of memory subsystem using SRAM and DRAM. Design of various I/O devices and systems. Design special purpose controllers

6. Prerequisite(s): CSE-121, CSE-122 and CSE-321

7. Course Designation as Elective or Required: Required

8. Course Objectives:

(a) Familiarization with the Digital System Design tools (VHDL, Xiling, etc.) and hardware equipment
(b) Introduce the concept of various component design and use them to design a digital computer
(c) Design and analyze a complete digital system by combining various components

9. Student Learning Outcomes: After successfully completing the course with a grade of D (2.0/4.0) or better, the student should be able to do the following

No.	Course Outcomes (COs)
1	Analyze the design principle of a digital system to decompose the whole system in various modules using modular approach
2	Design various Modules of a digital computer such as Adder, Arithmetic unit, ALU memory, processor, etc.
3	Implement and Analyze the design components using modern design tool (VHDL) and traditional hardware based system

10. Mapping of Program Outcomes Addressed by COs

CO-PO mapping

CO#	Program Outcome (PO)	PO#
1	**Problem analysis:** Identify, formulate, research literature and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences.	2
2	**Design/Development of solutions:** Design solutions for complex engineering problems and design systems, components or processes that meet specified needs with appropriate consideration for public health and safety, cultural, societal, and environmental considerations.	3
3	**Modern tool usage:** Create, select and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modelling, to complex engineering problems, with an understanding of the limitations.	5

CO—PO—WP—WA Mapping

No.	Title of Course	Programs Outcomes (PO)												Complex Engineering Problem Solving	Complex Engineering Activities
		Engineering Knowledge	Problem Analysis	Design	Investigation	Modern Tools	Engineers and Society	Environment and sustainability	Ethics	Teamwork	Communication	Project Management and Finance	Life-long Learning		
1.	CSE-423: Digital System Design (Theory)	×	×	×										×	
2.	CSE-424: Digital System Design (Sessional)		×	×		×								×	

Mapping of Complex engineering problem/ complex activities/knowledge profile

NO	COURSE CODE & TITLE	BLOOM`S TAXONOMY LEVEL	POs	COMPLEX PROBLEM SOLVING											COMPLEX ACTIVITIES					KNOWLEDGE PROFILE													
				WP1					WP2	WP3	WP4	WP5	WP6	WP7	EA1	EA2	EA3	EA4	EA5	PO1				PO2				PO3	PO4	PO5	PO6	PO7	PO8
				Depth of knowledge																													
				WK3	WK4	WK5	WK6	WK8												WK1	WK2	WK3	WK4	WK1	WK2	WK3	WK4	WK5	WK8	WK6	WK7	WK7	WK7
				ENGINEERING FUNDAMENTAL	SPECIALIST KNOWLEDGE	ENGINEERING DESIGN	ENGINEERING PRACTICE	RESEARCH LITERATURE	RANGE OF CONFLICTING	DEPTH OF ANALYSIS REQUIRED	FAMILIARITY OF ISSUES	EXTENSIVE APPLICABLE CODES	STAKEHOLDERS INVOLVEMENT & CONFLICTING REQUIREMENTS	INTERDEPENDENCE	RANGE OF RESOURCES	LEVEL OF INTERACTIONS	INNOVATIONS	CONSEQUENCES TO SOCIETY & ENVIRONMENT	FAMILIARITY OF ISSUES	NATURAL SCIENCES	MATHEMATICS	ENGINEERING FUNDAMENTAL	SPECIALIST KNOWLEDGE	NATURAL SCIENCES	MATHEMATICS	ENGINEERING FUNDAMENTAL	SPECIALIST KNOWLEDGE	ENGINEERING DESIGN	RESEARCH LITERATURE	ENGINEERING PRACTICE	COMPREHENSION	COMPREHENSION	COMPREHENSION
1	CSE-424: Digital System Design (Sessional)	C3, C4, A3, P3	2, 3, 5	X	X	X	X			X				X												X	X	X		X			

11. Assessment Strategy:

Mapping of Tasks with POs, WPs, WKs and EA

<table>
<tr><th>Possible tasks</th><th>Course Outcomes (CO)</th><th>Program Outcomes (PO)</th><th>Knowledge Profile (WK))</th><th>Complex Engineering Problem (WP)</th><th>Complex Engineering Activities (EA)</th></tr>
<tr><td>T-1: Decompose the whole design problem into sub problems using modular approach considering multiple solutions</td><td rowspan="2">CO-1</td><td rowspan="2">PO2: Problem Analysis</td><td rowspan="2">WK3
WK4</td><td rowspan="3">WP1: Depth of Knowledge

WP3: Depth of Analysis Required

WP7: Interdependence</td><td rowspan="3">N/A</td></tr>
<tr><td>T-2: Identify the specific requirements and constraints involved in designing each of the modules or sub problems</td></tr>
<tr><td>T-3: Design various Modules of a digital computer such as Adder, Arithmetic unit, ALU memory, processor, etc.</td><td>CO-2</td><td>PO3: Design/ Development Solutions</td><td>WK5</td></tr>
<tr><td>T-4: Use of modern tool in analysis and design of components</td><td>CO-4</td><td>PO5: Use of Modern Tools:</td><td>WK6</td></tr>
</table>

ASSESSMENT RUBRIC:

Task No.	Criteria	Assessment Tools	Exceptional	Acceptable	Marginal	Unacceptable
T-1	**Draw the block diagram and logic diagram of the system**	Report Quiz	Complete diagram of the system with valid logical reasoning that uses minimum number of components	Complete diagram of the system with valid logical reasoning that uses an acceptable level of redundancy	Complete diagram of the system with valid logical reasoning that uses a lot of redundancy	Complete diagram of the system with invalid logical reasoning
T-2	**Use of appropriate components**	Report & Quiz	Explore available alternatives and select appropriate components	Explore limited alternatives and select appropriate components	Explore limited alternatives and select complex components still serving the purpose	Explore limited alternatives and select inappropriate components
T-3	**Use of formal design procedure**	Report	Effective use of system design principles ensuring the desired objectives	Reasonable use of system design principles ensuring the desired objectives	No Effective use of system design principles still meeting the desired objectives	No Effective use of system design principles and fails to ensure the desired objectives
T-4	**Analyze the design using of software Tools**	Report & Lab Performance	Standard software tools are used effectively to develop and analyze the designs	Standard software tools are used with moderate effectiveness to develop and analyze the designs	Minimal application and use of Standard software tools	Inappropriate application and use of Standard software tools

Lesson Plan

`	Topic	Lesson Learning Outcomes and corresponding CO (at the end of the lesson students will be able to …)	Corresponding COs	Assessment Method
Week-01	Introduction to the Digital System Design Lab	• Lab orientation with safety instructions • Identify various devices and equipment of Digital System Design Lab • Install and use of VHDL software	NA	NA
Week -02	Introduction to VHDL	• Use VHSIC (very high speed integrated circuit) hardware description language (VHDL) to design digital system • Explain VHDL language concept and design methodology	NA	• Lab Report
Week -03	Implementation of Full Adder and parallel adder Circuit in Dataflow, Behavioral & Structural Design Process in VHDL	• Compare three different VHDL design methodology • Use the concept of modular approach in practical design • Simulate the design using ‘testbench’ to verify the input output relations	3	• Lab Report • Lab Performance (Individual)
Week -04	Implementation of Different Sequential Circuits in VHDL	• Compare the design requirements of combinational and sequential circuit • Simulate the design using ‘testbench’ to verify the input output relations	3	• Lab Report • Lab Performance (Individual)
Week -05	Implementation of a 4-bit Register and counter in VHDL	• Realize synchronization among various components of a complex system • Interconnect various time dependent components. • Simulate the design using ‘testbench’ to verify the input output relations	3	• Lab Report • Lab Performance (Individual)

Week -06	Implementation of register transfer statements in hardware	• Draw the block diagram/Logic diagram representation of the hardware • Identify appropriate LSI or MSI ICs for each block • Implement the design and analyze its operation.	1 & 2	• Lab Report • Lab Performance (Team)
Week -07	Design and Implementation of an 4-bit Arithmetic Circuit	• Use systematic design procedure to design an Arithmetic Circuit with given set of operation • Identify appropriate components (LSI or MSI ICs) for each block of the design • Implement the design in hardware as well as in VHDL and analyze its operation	1, 2 & 3	• Lab Report • Lab Performance (Team)
Week -08	Design and Implementation of an Arithmetic Logic Unit (ALU) in VHDL	• Use systematic design procedure to design an ALU with given set of operation • Identify appropriate VHDL design method • Implement the design in VHDL and analyze & synthesis the design for optimization	1, 2 & 3	• Lab Report • Lab Performance (Team)
Week -09	Design and Implementation of a 4-bit Combinational Shift Unit	• Use systematic design procedure to reduce the number of clock pulse with given set of operation • Identify appropriate components (LSI or MSI ICs) for each block of the design • Implement the design in hardware as well as in VHDL and analyze its operation	1, 2 & 3	• Lab Report • Lab Performance (Team)
Week -10	Performance test	• Individually solve **open-ended** hardware design problem using VHDL	1, 2 & 3	• Lab Performance (Individual)
Week -11	Viva-voce		NA	• Individual
Week -12	Quiz		NA	• Individual Test